Audio/Video, 60 MHz, 16 × 8, Gain of +2 Crosspoint Switch

AD8112

FEATURES

- Low cost, 16 × 8, high speed, nonblocking switch array
  - Pin-compatible 16 × 16 version available (AD8113)
- Serial or parallel programming of switch array
- Serial data out allows daisy chaining control of multiple 16 × 8 arrays to create larger switch arrays
- Output disable allows connection of multiple devices without loading the output bus
- Complete solution
  - Buffered inputs
  - 8 output amplifiers
  - Operates on ±5 V or ±12 V supplies
  - Low supply current of 54 mA
- Excellent audio performance V_S = ±12 V
  - ±10 V output swing
  - 0.002% THD at 20 kHz maximum 20 V p-p (R_L = 600 Ω)
- Excellent video performance V_S = ±5 V
  - 0.1 dB gain flatness of 10 MHz
  - 0.1% differential gain error (R_L = 1 kΩ)
  - 0.1° differential phase error (R_L = 1 kΩ)
- Excellent ac performance
  - −3 dB bandwidth 60 MHz
- Low all-hostile crosstalk of −83 dB at 20 kHz
- Reset pin allows disabling of all outputs (connected to a capacitor to ground provides power-on reset capability)
- 100-lead LQFP (14 mm × 14 mm)

APPLICATIONS

- CCTV surveillance/DVR
- Analog/digital audio routers
- Video routers (NTSC, PAL, S-Video, SECAM)
- Multimedia systems
- Video conferencing

FUNCTIONAL BLOCK DIAGRAM

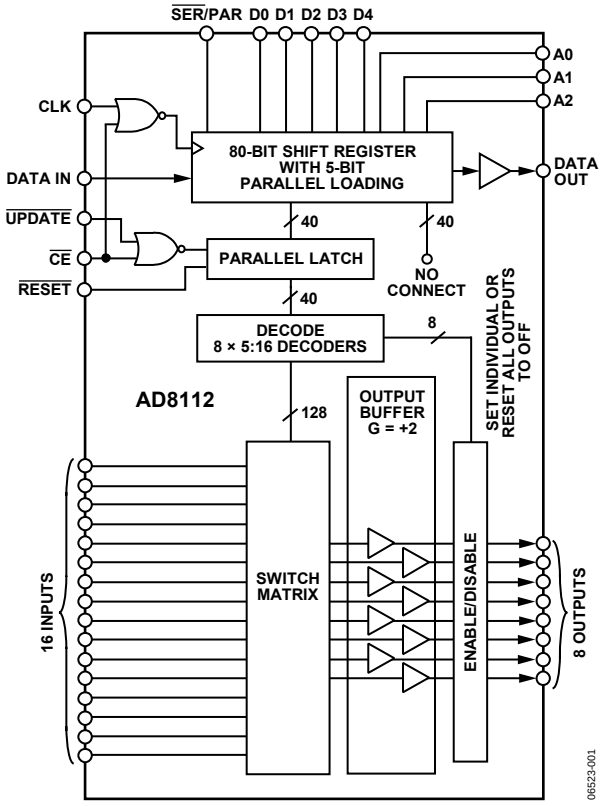

Figure 1.

GENERAL DESCRIPTION

The AD8112 is a low cost, fully buffered crosspoint switch matrix that operates on ±12 V for audio applications and ±5 V for video applications. It offers a −3 dB signal bandwidth greater than 60 MHz and channel switch times of less than 60 ns with 0.1% settling for use in both analog and digital audio. The AD8112 operated at 20 kHz has a crosstalk performance of −83 dB and isolation of 90 dB. In addition, ground/power pins surround all inputs and outputs to provide extra shielding for operation in the most demanding audio routing applications. With a differential gain and differential phase better than 0.1% and 0.1°, respectively, and a 0.1 dB flatness output of up to 10 MHz, the AD8112 is suitable for many video applications.

The AD8112 includes eight independent output buffers that can be placed into a disabled state for paralleling crosspoint outputs so that off channel loading is minimized. The AD8112 has a gain of +2. It operates on voltage supplies of ±5 V or ±12 V while consuming only 34 mA or 31 mA of current, respectively. The channel switching is performed via a serial digital control (which can accommodate the daisy chaining of several devices) or via a parallel control, allowing updating of an individual output without reprogramming the entire array.

The AD8112 is packaged in a 100-lead LQFP and is available over the commercial temperature range of 0°C to 70°C.

Rev. 0

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REVISION HISTORY

2/07—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = ±12 V, R_L = 600 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 200 mV p-p, R_L = 600 Ω, V_S = ±12 V	46	60		MHz
	V_{OUT} = 200 mV p-p, R_L = 150 Ω, V_S = ±5 V	41	60		MHz
	V_{OUT} = 8 V p-p, R_L = 600 Ω, V_S = ±12 V		10		MHz
	V_{OUT} = 2 V p-p, R_L = 150 Ω, V_S = ±5 V		25		MHz
Gain Flatness	0.1 dB, V_{OUT} = 200 mV p-p, R_L = 150 Ω, V_S = ±5 V		10		MHz
Propagation Delay	V_{OUT} = 2 V p-p, R_L = 150 Ω		20		ns
Settling Time	0.1%, 2 V Step, R_L = 150 Ω, V_S = ±5 V		23		ns
Slew Rate	2 V step, R_L = 150 Ω, V_S = ±5 V		100		V/µs
	20 V step, R_L = 600 Ω, V_S = ±12 V		120		V/µs
NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC, R_L = 1 kΩ, V_S = ±5 V		0.1		%
Differential Phase Error	NTSC, R_L = 1 kΩ, V_S = ±5 V		0.1		Degrees
Total Harmonic Distortion	20 kHz, R_L = 600 Ω, 20 V p-p		0.002		%
Crosstalk, All Hostile	f = 5 MHz, R_L = 150 Ω, V_S = ±5 V		−67		dB
	f = 20 kHz		−83		dB
Off Isolation	f = 5 MHz, R_L = 150 Ω, V_S = ±5 V, one channel		−100		dB
	f = 20 kHz, one channel		−83		dB
Input Voltage Noise	20 kHz		14		nV/√Hz
	0.1 MHz to 10 MHz		12		nV/√Hz
DC PERFORMANCE					
Gain Error	No load, V_S = ±12 V, V_{OUT} = ±8 V		0.3	2.5	%
	R_L = 600 Ω, V_S = ±12 V		0.5		%
	R_L = 150 Ω, V_S = ±5 V		0.5		%
Gain Matching	No load, channel-to-channel		0.7	3.5	%
	R_L = 600 Ω, channel-to-channel		0.7		%
	R_L = 150 Ω, channel-to-channel		0.7		%
Gain Temperature Coefficient			20		ppm/°C
OUTPUT CHARACTERISTICS					
Output Resistance	Enabled		0.3		Ω
	Disabled	3.4	4		kΩ
Output Capacitance	Disabled		5		pF
Output Voltage Swing	V_S = ±5 V, no load	±3.2	±3.5		V
	V_S = ±12 V, no load	±10.3	±10.5		V
	I_{OUT} = 20 mA, V_S = ±5 V	±2.7	±3		V
	I_{OUT} = 20 mA, V_S = ±12 V	±9.8	±10		V
Short-Circuit Current	R_L = 0 Ω		55		mA
INPUT CHARACTERISTICS					
Input Offset Voltage	All configurations		±4.5	±8.5	mV
	Temperature coefficient		10		µV/°C
Input Voltage Range	No load, V_S = ±5 V		±1.5		V
	V_S = ±12 V		±5.0		V
Input Capacitance	Any switch configuration		4		pF
Input Resistance			50		MΩ
Input Bias Current	Any number of enabled inputs	+1	±1.6		µA

Parameter	Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS					
Enable On Time			80		ns
Switching Time, 2 V Step	50% update to 1% settling		50		ns
Switching Transient (Glitch)			20		mV p-p
POWER SUPPLIES					
Supply Current	AV_{CC} outputs enabled, no load, V_S = ±12 V		50	54	mA
	AV_{CC} outputs disabled, V_S = ±12 V		34	38	mA
	AV_{CC} outputs enabled, no load, V_S = ±5 V		45	50	mA
	AV_{CC} outputs disabled, V_S = ±5 V		31	35	mA
	AV_{EE} outputs enabled, no load, V_S = ±12 V		50	54	mA
	AV_{EE} outputs disabled, V_S = ±12 V		34	38	mA
	AV_{EE} outputs enabled, no load, V_S = ±5 V		45	50	mA
	AV_{EE} outputs disabled, V_S = ±5 V		31	35	mA
	DV_{CC} outputs enabled, no load		8	13	mA
DYNAMIC PERFORMANCE					
Supply Voltage Range	AV_{CC}	4.5		12.6	V
	AV_{EE}	−12.6		−4.5	V
	DV_{CC}	4.5		5.5	V
PSRR	DC	75	80		dB
	f = 100 kHz		60		dB
	f = 1 MHz		40		dB
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (still air)		0 to 70		°C
θ_{JA}	Operating (still air)		40		°C/W

TIMING CHARACTERISTICS (SERIAL)

Table 2.

Parameter	Symbol	Limit Min	Limit Typ	Limit Max	Unit
Serial Data Setup Time	t_1	20			ns
CLK Pulse Width	t_2	100			ns
Serial Data Hold Time	t_3	20			ns
CLK Pulse Separation, Serial Mode	t_4	100			ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0			ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	50			ns
CLK to DATA OUT Valid, Serial Mode	t_7			200	ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off				50	ns
Data Load Time, CLK = 5 MHz, Serial Mode			16		µs
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times				100	ns
$\overline{\text{RESET}}$ Time				200	ns

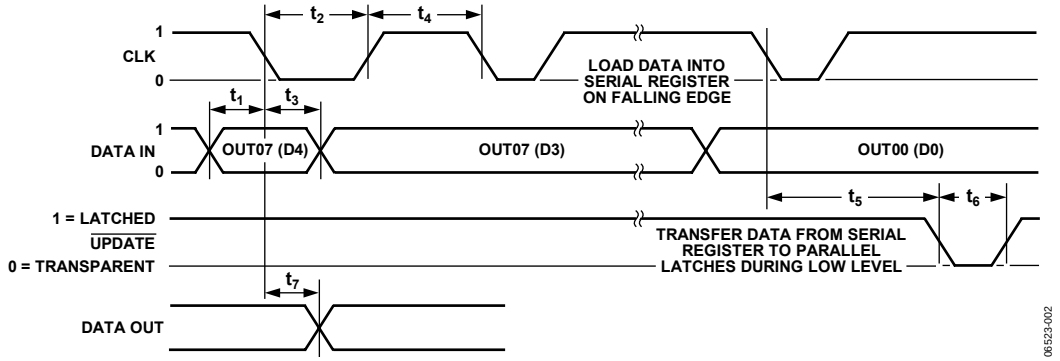

Figure 2. Timing Diagram, Serial Mode

Table 3. Logic Levels

Pins	V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	2.0 V min	0.8 V max			20 µA max	−400 µA min		
DATA OUT			2.7 V min	0.5 V max			−400 µA max	3.0 mA min

TIMING CHARACTERISTICS (PARALLEL)

Table 4.

Parameter	Symbol	Limit Min	Limit Max	Unit
Data Setup Time	t_1	20		ns
CLK Pulse Width	t_2	100		ns
Data Hold Time	t_3	20		ns
CLK Pulse Separation	t_4	100		ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0		ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	50		ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off			50	ns
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times			100	ns
$\overline{\text{RESET}}$ Time			200	ns

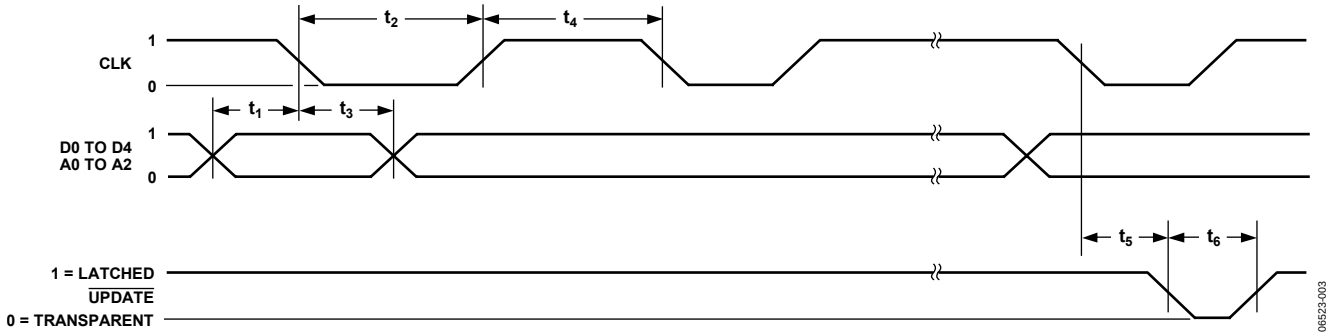

Figure 3. Timing Diagram, Parallel Mode

Table 5. Logic Levels

Pins	V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR, CLK, D0, D1, D2, D3, D4, A0, A1, A2, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	2.0 V min	0.8 V max			20 µA max	−400 µA min		
DATA OUT			2.7 V min	0.5 V max			−400 µA max	3.0 mA min

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Supply Voltage (AV_{CC} to AV_{EE})	26.0 V
Digital Supply Voltage (DV_{CC} to DGND)	6 V
Ground Potential Difference (AGND to DGND)	±0.5 V
Internal Power Dissipation[1]	3.1 W
Analog Input Voltage[2]	Maintain linear output
Digital Input Voltage	DV_{CC}
Output Voltage (Disabled Output)	(AV_{CC} − 1.5 V) to (AV_{EE} + 1.5 V)
Output Short-Circuit Duration	Momentary
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering 10 sec)	300°C

[1] Specification is for device in free air (T_A = 25°C): 100-lead plastic LQFP (ST): θ_{JA} = 40°C/W.
[2] To avoid differential input breakdown, ensure that one-half the output voltage (1/2 V_{OUT}) and any input voltage is less than 10 V of the potential differential. See Output Voltage Swing specification for linear output range.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

POWER DISSIPATION

The AD8112 is operated with ±5 V to ±12 V supplies and can drive loads down to 150 Ω (±5 V) or 600 Ω (±12 V), resulting in a large range of possible power dissipations. For this reason, extra care must be taken when derating the operating conditions based on ambient temperature.

Packaged in a 100-lead LQFP, the AD8112 junction-to-ambient thermal impedance (θ_{JA}) is 40°C/W. For long-term reliability, the maximum allowed junction temperature of the plastic encapsulated die should not exceed 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. The curve in Figure 4 shows the range of allowed power dissipations that meet these conditions over the commercial range of ambient temperatures.

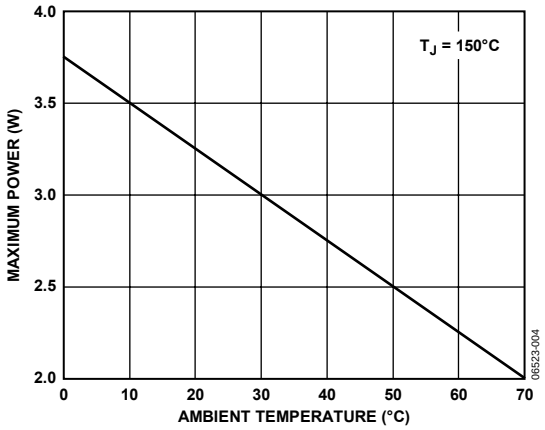

Figure 4. Maximum Power Dissipation vs. Ambient Temperature